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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/630,238	07/30/2003	Bart J. Van Zeghbroeck	50033-00006	8276

7590 09/30/2005

MARSH FISCHMANN & BREYFOGLE LLP
Suite 411
3151 South Vaughn Way
Aurora, CO 80014

EXAMINER	
VINH, LAN	

ART UNIT	PAPER NUMBER
1765	

DATE MAILED: 09/30/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/630,238	ZEGHBROECK ET AL.	
	Examiner	Art Unit	
	Lan Vinh	1765	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *30 July 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-25* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *13-25* is/are allowed.

6)☒ Claim(s) *1,3-5,8-12* is/are rejected.

7)☒ Claim(s) *2,6 and 7* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *110703*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claims 1, 3-5, 8-10 are rejected under 35 U.S.C. 103(a) as being unpatentable over Shor et al (US 6,034,004) in view of Lee (US 6,790,685)

Shor discloses a method for etching of silicon carbide semiconductor using selective etching. The method comprises the steps of:

providing a multi-layer laminate including at least layer 12a/first and second layer 11 of SiC/wide bandgap semiconductor material (col 3, lines 8-23)

masking the upper surface of layer 12 and maintaining the SiC layer at a potential (col 4, lines 5-8; lines 54-56), which reads on isolating an area of the first layer of semiconductor material for locating a conductance measurement device

measuring a first potential of 0.5 V/conductance of the masked layer/isolated area 12a/first layer of semiconductor material (col 6, lines 21-24)

first etching a first amount of the layer 12a/first layer of semiconductor material (col 7, lines 1-2)

measuring a second potential of 1.0 V/second conductance of the isolated area of layer 12a/the first layer of semiconductor material subsequent to etching the first amount of the first layer of semiconductor material (col 6, lines 24-25)

utilizing the first and second measured conductance to determine the dwell time/a time required to etch a second amount of the first layer of semiconductor material (col 6, lines 47-55)

Unlike the instant claimed invention as per claim 1, Shor fails to specifically disclose measuring a first potential /conductance of the isolated area of the semiconductor material using a conductance measuring device

Lee discloses a method for forming a test pattern comprises the step of measuring a voltage/conductance of the isolated area of the semiconductor material using a measuring line/conductance measuring device (col 5, lines 19-21)

Hence, one skilled in the art at the time the invention was made would have found it obvious to modify Shor method by measuring a first potential /conductance of the isolated area of the semiconductor material using a measuring line to measure voltage between nay two points of the semiconductor layer thereby forming a test pattern as taught by Lee (col 5, lines 22-24)

Regarding claim 3, Shor discloses the step of etch through/ second etching the first layer of semiconductor material for the determined amount of time to remove the second amount of the first layer of semiconductor material (col 7, lines 1-3)

Regarding claims 4, 10, fig. 5E of Shor shows layer 12a/first layer of semiconductor material is etched to a p-n junction between the first and second layer of semiconductor material

Regarding claim 5, fig. 5E shows that the etch through/ second etching removes a portion of layer 12a/first layer to achieve a thickness of the layer 12a/first layer

The limitation of claim 8 has been discussed above

3. Claims 11-12 are rejected under 35 U.S.C. 103(a) as being unpatentable over Shor et al (US 6,034,004) in view of Lee (US 6,790,685) and further in view of Temple (US 4,314,266)

Shor as modified by Lee has been described above. Unlike the instant claimed inventions as per claims 11-12, Shor and Lee fail to specifically disclose etching a semiconductor device such as a transistor/thyristor

Temple discloses a method for forming a thyristor having p-n junction (col 3, lines 19-23)

Since Shor is directed to a method of forming a device having a p-n junction, one skilled in the art at the time the invention was made would have found it obvious to employ Shor and Lee method to etch a semiconductor device such as a transistor/thyristor in view of Temple teaching because Temple discloses that a pn junction defines the boundary between the base and third zone of the thyristor/transistor (col 3, lines 29-31)

Allowable Subject Matter

4. Claims 13-25 allowed.

The following is an examiner's statement of reasons for allowance:

Regarding claim 13, the cited prior art of record, taken alone or in combination, fails to disclose a method for precisely etching a wide bandgap semiconductor device

comprises the step of repeating the step of first etching the first layer of semiconductor material a first amount and the step of measuring a second conductance of the first layer of semiconductor material etched the first amount to determine an optimal time to etch the first layer of semiconductor material a second amount, in combination with the rest of the limitations of claim 13

Claims 2, 6-7 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Conclusion

5. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Lan Vinh whose telephone number is 571 272 1471. The examiner can normally be reached on M-F 8:30-5:30 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Nadine Norton can be reached on 571 272 1465. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

LV
September 26, 2005